10. The phase detector circuit of claim 8, wherein said second signal is the same as said input random NRZ signal but differing in phase therefrom by an angle θ, and said delay circuit delays said input random NRZ signal by a value of (T-δT), where δT is a value less than T.

11. The phase detector circuit of claim 8, wherein said second signal is a clock signal derived from said input random NRZ signal but differing in phase therefrom by an angle θ, and said delay circuit comprises a latch circuit that is clocked by said clock signal.

12. The phase detector circuit of claim 8, wherein said delay circuit comprises a first voltage-controlled delay circuit and a control circuit for controlling said voltage-controlled delay circuit.

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13. The phase detector circuit of claim 12, wherein said control circuit comprises an oscillator for outputting a clock signal having the same period as said input random NRZ signal, a second voltage-controlled delay circuit that receives said clock signal and outputs a delayed version of said clock signal in accordance with a control signal, a phase difference detector for detecting a phase difference between said clock signal and said delayed version of said clock signal and outputting said detected phase difference to a low pass filter, which low pass filter outputs said control signal to said first and second voltage-controlled delay circuits.

14. The phase detector circuit of claim 9, wherein said combination comprises a first multiplier circuit for multiplying said input random NRZ signal with said second signal, a second multiplier circuit for multiplying said second signal with the output of said delay circuit, and said subtractor circuit subtracts the output of said second multiplier circuit from the output of said first multiplier circuit.

15. A phase detector circuit that outputs a DC voltage signal associated with a phase difference between an input random NRZ signal and a second signal related to said input random NRZ signal, comprising: